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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,465	12/28/2000	Calvin Guey	JCLA6707	6593

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EXAMINER
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ART UNIT	PAPER NUMBER
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,465	GUEY ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/28/00, 3/12/01,9/14/01, 2/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *1 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Receipt is acknowledged of the following papers:

1) Priority papers (3/12/01)

2) Change of address (9/14/01)

3) Change of address (2/24/01)

These papers have been placed of record in the file.

2. Claims 1-6 have been examined.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Drawings

4. The drawings are objected to because

1) In Fig. 1, the element 140 is incorrectly labeled as "Address Counter". With respect to the claims, it should be "Address Calculator".

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

1) On pg. 7, line 5, the specification incorrectly refers to element 160 of Fig. 1 as "register address list" instead of "register list".

Appropriate correction is required.

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: APPARATUS AND METHOD FOR EXECUTING AN INSTRUCTION WITH A REGISTER BIT MASK FOR TRANSFERRING DATA BETWEEN A PLURALITY OF REGISTERS AND MEMORY INSIDE A PROCESSOR.

7. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

8. An abstract, which provides a more unambiguous concise statement of the technical disclosure, is requested.

Claim Objections

9. Claim 1 is objected to because of the following informalities:

1) On pg. 10, line 15, it is recommended to change the words "having the corresponding" to "that correspond to the" to properly reflect the invention.

Appropriate correction is requested.

10. Claim 4 is objected to because of the following informalities:

1) On pg. 11, line 9, the action of "linking up" is not very clear. For the purposes of the following art rejection, it is interpreted as a form of "mapping" the plurality of registers to the memory unit.

Appropriate correction is requested.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Higaki et al (US005796970A).

13. In regard to Claim 4:

14. Higaki et al. disclose a method of executing a block data transfer instruction ("MOVEM" instruction, col. 1, line 28) inside a processor (col. 1, line 33) after receiving decode information (Fig. 4, Register Designating field) containing N bits (Fig. 2, shows the register designating field with 8 bits; col. 1, line 62, indicates that the field can be of N bits), comprising the steps of :

1) adding (Fig. 4, element 214, number of register detection circuit; Fig. 6D shows a truth table for the circuit which indicates that it performs adding) the N bits together to form an initial count value (Fig. 6D, output column 1; col. 7, line 65-66);

2) generating a plurality of register identification number (a register identification number generator, Fig. 4, 202, 204) identical in number to the initial count value, wherein the register identification number corresponds to the bit position of the N-bit decode information that has a bit value '1'(col. 6, lines 4-8, 36-50);

3) linking up (mapping) the plurality of registers that correspond to the register identification numbers and the memory unit according to the register identification numbers (the instruction decoder Fig. 3, 101, col. 5, lines 17-22, controls the transfer of data between the registers that correspond to the register identification numbers which are successively output by the register designating field decoder, 105, and the memory 104 wherein the address calculator, Fig. 3, 103, col. 5, lines 32-39, successively calculates memory addresses each time register data is transferred based on the control by the instruction decoder) so that stored data can be exchanged between memory unit and the registers.

15. In regard to Claim 6:

16. Higaki et al. further disclose a method which includes generating an address signal (calculator group, Fig. 3, 103, col. 5, lines 27-39) according to the decode information so that stored data in the register corresponding to the register identification number and data within the memory unit having an address corresponding to the address signal can exchange with each other.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1, 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higaki et al (US005796970A).

19. In regard to Claim 1:

20. Higaki et al. disclose an apparatus (col. 1, line 47) for executing block data transfer instruction ("MOVEM" instruction, col. 1, line 28) inside a processor (col. 1, line 33) after receiving decode information (Fig. 4, Register Designating field) containing N bits (Fig. 2, shows the register designating field with 8 bits; col. 1, line 62, indicates that the field can be of N bits), the apparatus comprising:

1) an adder (Fig. 4, element 214, number of register detection circuit; Fig. 6D shows a truth table for the circuit which indicates that it is an adder) for receiving the N-bit decode information (col. 7, line 60) and adding the N bits together to produce an initial count value (Fig. 6D, output column 1; col. 7, line 65-66);

2) a register identification number generator (Fig. 4, 202, 204) that generates a plurality of register identification numbers (Fig. 4, d) equal in number to the initial count value, wherein the register identification number corresponds to the bit positions in the N-bit decode information having a bit value '1' (col. 6, lines 4-8, 36-50);

3) a memory unit (Fig. 3, 104, col. 5, lines 40-41) for holding data;

4) a register list (Fig. 3, 102) that includes a plurality of registers (col. 5, lines 23-24), wherein the register list is able to receive the register identification numbers (Fig. 3, output of 105) so that the stored data can be freely exchanged between the memory unit and the registers that correspond to the register identification numbers.

21. The apparatus disclosed by Higaki et al. differs from the present invention because it does not have a counter for receiving the initial count value, which decreases the value by one after outputting a count control signal.

22. Higaki et al. disclose a register processing continuation signal (Fig. 4, output of the register processing completion detection circuit, 211) which is set to a "1" (valid) while all the registers designated to be transferred are being processed (col. 7, lines 44-47). One of ordinary skill in the art would have recognized that one could simplify the Higaki et al. circuit by removing the group register transfer circuitry and use a down counter which counts down from the initial count value to indicate that register processing is continuing and when it reaches zero, indicate that the transfer is complete.

23. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a counter for receiving the initial count value and indicate the end of data transfer in the apparatus disclosed by Higaki et al.

24. In regard to Claim 2:

25. Higaki et al. teach an address calculator (Fig. 3, 103, col. 5, lines 27-39) for generating an address signal according to the decode information and then outputting the address signal to the memory unit so that data can be freely exchanged between the registers that correspond to the register identification numbers and the addressed memory in the memory unit according to the address signal.

26. In regard to Claim 5:

27. Higaki et al. further teach a method wherein the step for generating the register identification numbers includes the sub-step of generating a register identification number whenever a bit value '1' is found in the N-bit decode information (col. 6, lines 4-8, 36-39).

28. The method taught by Higaki et al. differs from the present invention because it does not disclose performing a count down operation decreasing the initial value count by one until the value zero is reached and of generating the register identification number after each count down operation.

29. However it would have been obvious to one of ordinary skill in the art at the time of the invention to have performed the count down operation to indicate the end of the transfer between the register list and memory and be given as an input to the register processing completion detection circuit (Fig. 4, element 211; col. 7, lines 40-47), which controls the clock input to the instruction register (Fig. 4, element 100) and allows it to start fetching again (col. 7, lines 48-50). Also a person of ordinary skill in the art would have recognized at the time of the invention that a register identification number could be generated after each count down operation, hence when the counter would reduce to zero it would indicate to stop generating register identification numbers and this work as a control signal.

30. Hence it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method disclosed by Higaki et al., by including the steps of performing a count down operation and generating the register identification number after each count down operation.

31. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higaki et al. as applied to claim 1 above, and further in view of McAlister et al. (US004348741).

32. Higaki et al. teaches that the register identification number generator (Fig. 4, 202 [priority encoder], 204) for generating register identification numbers equal in number to the initial count value, is able to generate corresponding register identification number according to the bit position (col. 6, lines 36-39) in the N-bit (Fig. 2, shows the register designating field with 8 bits; col. 1, line 62, indicates that the field can be of N bits) decode information that has a value '1' (col. 6, lines 4-8).

33. Higaki et al. do not teach that the register identification number generator includes N logic units and that when the counter decrements by one down to zero, the N logic unit is able to generate the corresponding register identification number according to the bit position in the N-bit decode information that has a value one.

34. McAlister et al. teach a priority encoder which is simple, fast, and occupies less space on chip (col. 2, lines 35-37). It has 16 units (Fig. 2) for a 16-bit input.

35. One of ordinary skill in the art at the time of the invention would have motivated to use the priority encoder taught by McAlister et al. to implement the priority encoder, 202, of Higaki et al. for register identification number generation as it is a simple, fast, and smaller size (col. 2, lines 35-37).

36. Also, it would have been obvious to one of ordinary skill in the art to use a counter, which contains the initial count value (number of registers to be transferred), in the Higaki et al. apparatus to indicate the end of the register processing/transfer by decrementing it by one every time a register identification number is sent to the register list. Hence, when such a counter decrements by one down to zero, the N logic unit is able to generate corresponding register identification number.

37. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to use the priority encoder as taught by McAlister having N units for a corresponding N bit input and to use the counter such that as it decrements by one down to zero, the N logic unit of the register is able to generate corresponding register identification number.

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty, which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections. See 37 CFR § 1.111.

a. Fiene et al. (US005265258A) disclose a priority encoder circuit for the MOVEM instruction of the MC68000 instruction set.

b. MC68030, Enhanced 32-bit microprocessor user's manual by Motorola, published by Prentice-Hall, 1989, discloses the MOVEM instruction which moves data between multiple registers and memory.

c. Zolnowsky et al. (US004729094) disclose a multiple register transfer instruction (Fig. 7, Evaluate EA and transfer multiple CP registers, col. 21, lines 30-60). It teaches of determining which registers to transfer based on the selected bits in a selector mask. It also teaches that the processor counts the bits to determine the number of registers to be transferred.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

AVG

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